REMARKS

This responds to the final Office Action mailed on December 3, 2003.

§102 Rejection of the Claims

Claim 1 was rejected under 35 U.S.C. § 102(b) as being anticipated by Huang et al. (U.S. 5,719,088). This rejection is respectfully traversed.

A passivation layer, as used in the present application, alters the electronic properties of the surface of the transistor. The function of the AlN passivation layer is to stop the uncontrolled changing of charge states at the surface during the operation of the transistor. These charge states may be due to dangling bonds, impurities, or other defects. The surface states are being controlled by this layer to be electronically passive, in contrast to being uncontrollably active.

Page 9, lines 13-15 of the application states: "One theory of the effect of surface nitrides deposited on HFETs is that the most important aspect of surface coverage is to better confine the electrical extension of the gate along the surface." The application describes the layer as changing the electrical properties, not protecting layers below from etching.

Huang et al. indicates that layer 25 is AlN, but this is never used as a passivation layer, it is only used as an etch stop layer. As such, it is a process tool. No other functions are ascribed to it. In fact, Huang et al. indicates specifically that silicon nitride layer 22 is the passivation layer in Column 3, lines 5-15. This teaches away from having AlN function as a passivation layer. There is no stated reason to have two passivation layers.

While the function of the AlN passivation layer in each of the pending claims should be sufficient to distinguish Huang et al, there are further differences. In claim 1, the passivation layer is formed on the top surface of the heterojunction channel field effect transistor, not on top of other layers as shown in Huang et al. In Huang et al., the AlN etch stop is formed on top of the actual passivation layer, not on a top surface of the transistor as claimed. Thus, it cannot accomplish the function of better confining the electrical extension of the gate along the surface.

Huang et al., also mentions a passivating film 35 that is formed at the same time that layer 22 is etched. Col. 4, lines 20-34. Thus, Huang et al. clearly distinguishes an insulating

layer or etch stop layer from a passivating layer. The AlN layer of Huang et la. is clearly not a passivating layer as claimed.

In the response to arguments section of the final office action, the Examiner indicates that Huang et al. refers to the AlN layer as an intermediate protective or passivation layer for layers below during an etching process. However, there is no express reference to the AlN layer as a passivation layer. While it may function to reduce "the possibility of incidental damage", it does not provide the type of passivation defined and claimed in the present application. Thus, it is not a passivation layer within the meaning of the current claims.

The Examiner also mentions that in FIG. 2 of Huang et al., the AlN layer 25 is formed on a top surface of the HFET. However, FIG. 2 refers to an intermediate step in the formation of the HFET. Further, the AlN layer is formed over an insulating layer 22. The Examiner indicates that the passivation layer 32 is expressly shown as an intermediate passivation layer of HFET 10 in the current application. This is not correct. Perhaps the Examiner is indicating that the airbridge is part of the HFET. This is not the case. Passivation layer 32 is clearly formed on top of the active components of the HFET.

Further, the Examiner indicates that the present application uses passivation layer 32 as an etch stop during the etching or patterning process of resist layer 64. This is respectfully traversed, as the application clearly states that "After forming the passivation layer 32, photoresist is deposited and patterned to form an etch mask 64 defining windows in the passivation layer for electrical connections as illustrated in Figure 7." Page 7, lines 22-24. It is clear that the passivation layer 32 is not an etch stop. In fact, passivation layer 32 is expressly etched where not covered by the photoresist to form windows in it.

§103 Rejection of the Claims

Claims 2 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Huang et al. in view of Yoshida (U.S. 6,281,099). Claim 2 should be allowable since it depends from claim 1, which is now believed allowable. Yoshida does not add anything to Huang et al. that is lacking with respect to claim 1. Yoshida seems to be forming single crystal AlN for different purposes, such as for a semiconductor material for forming devices, forming a high hardness

layer, and for use in large area surface displays. It does not address the same problems solved by the present claims, and hence is not properly combinable with Huang et al.

Claims 3 and 4 were rejected under 35 USC § 103(a) as being unpatentable over Huang et al. in view of Kato et al. (U.S. 6,069,020). Claims 3 and 4 should be allowable since they depend from claim 1, which is now believed allowable. While Kato et al. does mention that layer 2A is GaAs (a III-V compound), there is no teaching that AlN may be deposited in the same manner as GaAs. Most of the teaching of the application is with respect to forming II-VI compounds. FIG. 2 is also an incorrect figure. It appears to be a circuit diagram, while the application refers to it as a structural diagram of an MBE apparatus.

The Office Action also indicates that "it should be inherent that such process comprises delaying a predetermined amount of time between each alternative application." Inherency is referenced in MPEP § 2112: "In relying upon the theory of inherency, the examiner must provide basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art," citing Ex parte Levy, 17 USPQ2d 1461, 1464 (Bd. Pat. App. & Inter. 1990) (emphasis in original). The Office Action contains no assertion that delaying a predetermined amount of time necessarily flows from the description of Kato et al., other than an assumption that perhaps there is only one molecular beam source which must be switched between targets, when in fact Kato et al. specifically recites multiple such sources 37. Therefore, a prima facie case of inherency has not been established, and the rejection should be withdrawn.

Further, Kato et al. specifically refers to using the beams simultaneously. Therefore, there is no requirement that there be a time period between alternate applications of the beams, since Kato et al., is capable of operating them at the same time. In fact, inserting a delay between alternating the beams would only add to the thermal budget of the device being formed. Absent such teaching, one possible assumption is that the beams are applied alternately with no time between switching the beams. Thus, the rejection should be withdrawn.

Claims 5 and 9 were rejected under 35 USC § 103(a) as being unpatentable over Huang et al. in view of Yoshida (U.S. 6,281,099). This rejection is respectfully traversed. Claim 5 is an independent claim that distinguishes Huang for at least the same reasons as claim 1. Claim 9

should be allowable since it depends from claim 5, which is now believed allowable. Yoshida does not add anything to Huang et al. that is lacking with respect to claim 1.

Claims 6-8 and 10-19 were rejected under 35 USC § 103(a) as being unpatentable over Huang et al. in view of Yoshida as applied to claim 5 above, and further in view of Kato et al. (U.S. 6,069,020). This rejection is respectfully traversed. Claims 6-8 depend from claim 5 which is now believed allowable. In addition, claims 7 and 8 specifically refer to delaying between the alternating beams, which is not inherent in Kato et al.

Claim 10 also depends from claim 5, and includes a further recitation that the beams are applied at a fairly low temperature, 150°C, that is commonly lower than that used for MBE. It should also be noted that low substrate temperatures are required for post device passivation. The present method may be performed at such low temperatures. Yoshida recites temperatures of the substrate of 500°C to 1500°C at Col. 3, lines 36-37, indicating that using MBE to form AlN would not be considered for forming a passivation layer. Claim 16 contains the same temperature, and should also be allowed. It is not merely a design choice. The low temperature is a result of the inventive process, that allows the formation of a passivation layer that was previously unattainable. The MBE in Kato et al. is only mentioned as being performed with the substrate at a desired temperature. The art cited in this application make it clear that such a desired temperature is well above 150°C.

Independent claim 11 recites alternating beams of Al and remote plasma nitrogen. None of the cited references teach this method. As indicated above, Kato et al. contains no teaching that AlN may be deposited in the same manner as GaAs. Most of the teaching of the application is with respect to forming II-VI compounds. Ratios for the VI/II compound are discussed in detail following the language about alternating beams in column 5, but there is no reference to the ratio of the GaAs compound. Therefore, it is tenuous at best that the GaAs is deposited in the same manner as the II/VI compounds. There is also no teaching in Kato et al. that AlN may be deposited in the same manner. FIG. 2 is also an incorrect figure. It appears to be a circuit diagram, while the application refers to it as a structural diagram of an MBE apparatus. Thus, the reference itself may not be enabling.

Claims 12-16 depend from claim 11, and distinguish the references for at least the same reasons. Claims 12-14 reference a delay, which is not inherent in Kato et al., and hence not

taught in any of the references cited. Claim 16, as indicated above, reference a temperature of 150°C, which is also far from any temperatures taught in the art. The temperature is meant to be an approximation of a temperature that would not adversely affect previously formed devices.

Claims 17-19 recite using MBE at a temperature of less than approximately 300°C. As indicated above with respect to claim 10 and 16, the art references a temperature much higher than this temperature, thus teaching away from use of MBE to form an AlN layer. Claim 17 also references waiting a predetermined period between applying alternate beams. This element is also not shown in the art cited, and the rejection should be withdrawn.

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney (612) 373-6972 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

WILLIAM J. SCHAFF ET AL.

By their Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. Box 2938
Minneapolis, MN 55402
(612) 373-6972

Date 2-3-2004 By _____
Bradley A. Forrest
Reg. No. 30,837

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Mail Stop AF, Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 3d day of February, 2004.

Dawn M. Poole _____
Name Signature